AMENDMENTS TO THE SUBSTITUTE SPECIFICATION

Please replace the paragraph at page 67, line 24, with the following rewritten paragraph:

Further, since the upper electrode and the lower electrode are arranged with shifting to each other along the first ~~directionD1~~ direction D1, only a portion which is stable in this film quality in the vicinity the electrode center, except for the vicinity of the electrode edges, is employed for a ferroelectric capacitor area, thereby realizing a capacitance element of stable characteristics.

Please replace the paragraph at page 83, line 15, with the following rewritten paragraph:

In addition, by reducing the dimension of the lower electrode 2n in the horizontal direction D1, the problems such as a short circuit between the different lower electrodes 2 can be overcome ~~or suppressed~~ in the manufacturing process.

Please replace the paragraph at page 84, line 20, with the following rewritten paragraph:

To be more specific, a memory cell capacitor 117a according to the seventeenth embodiment consists of a lower electrode 2 that is formed on a substrate (not shown) via an insulating film (not shown), a base electrode layer 5 that is formed in a groove extending over the plural lower electrodes 2 and on the circumference area, a ferroelectric layer 3q that is formed on the base electrode layer 5, and an upper electrode 4m that is formed on the ferroelectric layer 3q. Here, the dimensions of the lower electrode 2 in the horizontal direction D1 and the vertical direction D2 are the same as those of the base electrode layer 5 in the horizontal direction D1 and the vertical direction D2, respectively. Further, the dimension of the upper electrode 4m in the horizontal direction D1 is the same as the dimension of the ~~lower electrode 4m~~ lower electrode 2 in the horizontal direction D1. The ferroelectric layer 3q extends over the entire memory cell array both in the horizontal direction D1 and the vertical direction D2.

Please replace the paragraph at page 93, line 18, with the following rewritten paragraph:

An interlayer insulating film is formed thereon, then a groove is formed in the interlayer insulating film along the ~~vertical~~ horizontal direction D1 so as to reach the lower electrodes, and then a base electrode layer for three-dimensional structure is formed thereon. The base electrode layer is processed into the same rectangular shapes as the lower electrode 2s, thereby forming the base electrode layer 5s.

Please replace the paragraph at page 96, line 5, with the following rewritten paragraph:

More specifically, a memory cell capacitor 120 according to the twentieth embodiment consists of a lower electrode 2n that is formed on a substrate (not shown) via an insulating film (not shown), a base electrode layer 5r that is formed in a groove on the lower electrode 2n and on the circumference area, a ferroelectric layer 3t that is formed on the base electrode layer 5r, and an ~~upper electrode 4t~~ upper electrode 4r that is formed on the ferroelectric layer 3t. Here, the dimension of the lower electrode 2n in the horizontal direction D1 is smaller than the dimension of the base electrode layer 5r in the horizontal direction D1, and the dimension of the lower electrode 2n in the vertical direction D2 is the same as the dimension of the base electrode layer 5r in the vertical direction D2. The dimension of the lower electrode 2n in the horizontal direction D1 is smaller than the dimension of the ferroelectric layer 3t in the horizontal direction D1.